## REMARKS

Reconsideration of the application is respectfully requested for the following reasons:

Claims 1-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gardner et al. (US Patent No. 6,130,454 A) in view of Hsu et al. (US Patent No. 6,221,767 B1) and Brigham et al. (US Patent No. 5,714,413). The Examiner asserted in the Office Action that Gardner et al. discloses the following process steps: providing a wafer, wherein said wafer comprises a substrate (10); forming a trench (20) in said substrate; forming a gate (40) on a bottom of said trench; forming a spacer (46) on both sides of said gate and filling of said trench; implanting an ion into said substrate which is on both sides of said spacer; proceeding a first rapid thermal process to form a source/drain region (50) and a source/drain extended region (48) in said substrate; forming a metal layer on said gate, said spacer, and said source /drain region (see figure 12 and 8, lines 59-67); proceeding a second rapid thermal process to form a silicide layer on said gate and said source/drain region. The Examiner thinks that although Gardner el al. fails to teach the activation of source/drain implanted ions is done by rapid heating as recited in present claims 1 and 9, it is well-known to one skilled in the art that rapid heating has been used in activating ion implanted regions because rapid heating reduces the unwanted heat

exposure to the device. The Examiner also thinks that although Gardner el al. fails to explicitly teach the removal of unreacted metal after the silicidation process as recited in present 1 and 9, Hsu teaches that unreacted metal that is formed during the silicon process is removed. The Examiner further thinks that although Gardner el al. fails to teach that the silicide layer is formed by two rapid thermal treatments and the unreacted metal is removed as recited in present 9, Hsu teaches that a silicide layer is formed by two rapid thermal treatments and the unreacted metal is removed.

Gardner et al. merely discloses that a process is provided for forming a gate conductor within a trench having opposed sidewalls which approach each other as they pass from the upper surface of a semiconductor substrate to the floor of the trench. According to an embodiment, an opening is formed through a masking layer residing upon the substrate to expose the portion of the substrate to be etched during trench formation. The opening is created using optical lithography and an etch technique. As such, the minimum width of the opening is limited in size. Once the trench has been etched in the substrate, dielectric sidewall spacers may be formed upon the sidewalls of the trench and the lateral boundaries of the masking layer. A gate conductor is subsequently formed between the sidewall spacers. The lateral width of the resulting gate conductor is thus dictated by the distance between the sidewall spacers, and hence by the thickness of the spacer material deposited upon the sidewalls of the trench. The

spacers may be subsequently removed, and a relatively thick oxide layer may be formed upon the slanted trench sidewalls. The nitride layer may be removed, and dopant species may be implanted into the substrate exclusive of underneath the gate conductor. In this manner, LDD areas are formed proximate the trench sidewalls while source and drain regions are formed proximate the horizontal surface of the substrate.

Hsu et al. merely discloses that a method for fabricating a landing pad is described in which a transistor is formed on the substrate, wherein the transistor comprises a gate and source/drain regions at both sides of the gate in the substrate. A cap layer and a spacer are formed on the gate and at the sidewall of the gate respectively. A protective layer is formed to cover the substrate. The protective layer is then defined to form an opening to expose the source/drain region. A polysilicon landing pad is then formed in the opening and on the protective layer at the periphery of the opening. Silicidation is then conducted on the polysilicon landing pad to form a metal silicide landing pad and to destroy any native oxide at the source/drain region.

Brigham et al. merely discloses that a transistor comprises a deposited dual-layer spacer structure and method of fabrication. A

polysilicon layer is deposited over a gate dielectric, and is subsequently etched to form the polysilicon gate electrode of the transistor. Next, oxide is deposited over the surface of the gate electrode, followed by deposition of a second dielectric layer. Spacers are then formed adjacent to the gate electrode by etching back the second dielectric layer using a substantially anisotropic etch which etches the second dielectric layer faster than it etches the oxide.

The rejection is respectfully traversed because Gardner et al. discloses a method for forming a metal oxide semiconductor in a trench that is in the substrate. The lightly doped drain (LDD) region is used in Gardner et al. to avoid the short channel effect. The lightly doped drain region is formed by implanting drain ions into the substrate and passing through a annealing process after forming source/drain region. In the present invention, the source/drain extended region is used to replace the lightly doped drain region to avoid the short channel effect. After implanting ions into the source/drain region and passing through an annealing process, the source/drain region and the source/drain extended region of the present invention are formed at the same time and there is not any ion implanted into the source/drain extended region in the forming source/drain extended region process. Because the ions of the lightly doped region will diffuse to other regions to extend the lightly doped

drain region and to produce the short channel effect more easily in the following high temperature process, the lightly doped drain region is not suitable for smaller semiconductor element. Using the method of the present invention to form a metal oxide semiconductor in the trench that is formed in the substrate and use the source/drain extended region to replace the traditional lightly doped drain region can avoid the short channel effect more effectively and increase the efficiency of the semiconductor element. In order to control the diffusion region of the source/drain extended region of the present invention, the temperature range of the rapid thermal process that is used to form the source/drain region and the source/drain extended region is important to avoid forming the over-diffusion source/drain extended region that will cause the short channel effect. The present invention further limits that the depth range of the trench is about 50% to 80% of the thickness of the gate (referring to page 6, line 16 to 17). When the depth of the trench is less than 50% of the thickness of the gate, the junction depth of the source/drain is decreased at the same time and the series resistance is increased. This condition will decrease performance of the device of the present invention. When the depth of the trench is higher than 80% of the thickness of the gate, the bridge effect is produced in the source/drain region and the gate to cause the device of the present invention fail. Therefore, the present invention is different from the citation Gardner et al.

Although Hsu et al. discloses that the silicide layer is formed by using two rapid thermal processes and the unreacted metal layer is removed in the following process, the lightly doped drain is still used in Hsu et al. to avoid the short channel effect and is different from the source/drain extended region of the present invention.

According to the above, the result which combines Gardner et al. and Hsu et al. results in a common MOS which is formed in the trench that is formed in the substrate and comprises a lightly doped drain region to avoid a short channel effect. But this result cannot get the source/drain extended region that is used to replace the lightly doped drain region of the present invention in the smaller size semiconductor element. Therefore, the present invention is different from the result which combines Gardner et al. and Hsu et al.

With respect to the dependent claims, they not only include patentable features as claimed in the corresponding independent claims, but also possess their specific limitations.

It is therefore respectfully submitted that Claims 1-18 are patentable over the citation Gardner et al., Hsu et al., and Brigham et al., under 35 U.S.C. §103(a).

Conclusion

Having thus overcome each of the rejections made in this Office Action, withdrawal of the rejections and expedited passage of the application to issue is requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

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## VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claim 1 has been amended as follows:

1. (Amended) A method for forming a MOSFET, said method comprises:

providing a wafer, wherein said wafer comprises a substrate;

forming a trench in said substrate;

forming a gate on a bottom of said trench;

forming a spacer on both sides of said gate and filling of said trench;

implanting a ion into said substrate which is on both sides of said spacer;

proceeding a first rapid thermal process to form a source/drain region and a source/drain extended region in said substrate;

forming a metal layer on said gate, said spacer, and said source /drain region;

proceeding a second rapid thermal process to form a silicide layer on said gate and said source/drain region; and

removing said unreacted metal layer.

Claim 9 has been amended as follows:

9. (Amended) A method for forming a MOSFET, said method comprises:

providing a wafer, wherein said wafer comprises a substrate;

forming a trench in said substrate;

forming a gate on a bottom of said trench, wherein said gate comprises a gate oxide layer;

forming a spacer on a sidewall of said gate and said gate oxide layer and filling of said trench;

implanting a ion into said substrate which is on both sides of said spacer;

proceeding a first rapid thermal process to form a source/drain region and a source/drain extended region in said substrate;

forming a metal layer on said gate, said spacer, and said source /drain region;

proceeding a second rapid thermal process to form a silicide layer on said gate and said source/drain region; and

removing said unreacted metal layer and proceeding a third rapid thermal process.